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DOCUMENT-IDENTIFIER: US 5255322 A
TITLE: Multi-zone audio distribution amplifier

DEPR:
FIG. 2 illustrates the back panel 16 connected to an amplifier card 30. The amplifier card 30 includes a printed circuit board 32, with various amplifier components 34 thereon, and an air-cooled finned heat sink 36 attached to the circuit board 32 via bolts 38. The heat sink 36 is used to dissipate heat from the amplifier chip, discussed infra in connection with FIG. 3.

United States Patent [PT] United States Patent Office
Perkins et al. No. Patent Number 5,255,322
(c) Date of Patent Oct. 19, 1993

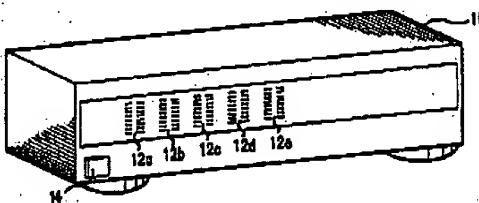
[1] INVENTOR: Robert P. Perkins, Larchmont, N.Y.;
Mark R. Ross, Greenwich, Connecticut; Michael Morgan, Parkville, both of Texas.
[2] APPLICANT: Rogers D Co., Paterson, NJ.
[3] Appl. No. 08/087,097
[4] Filed: Jan. 6, 1993
[5] Int. Cl.: F03D 7/00
U.S. Cl.: 365/102, 365/103, 365/104, 365/105
[6] Prior art cited:

4,681,146 1/27/91 Bassett H1/11
4,681,151 1/27/91 March H1/11
4,681,152 1/27/91 Dethlefsen et al. H1/11
4,681,153 1/27/91 Ferguson et al. H1/11

[7] OTHER PUBLICATIONS:
SD Products, Inc. & Powersys V.

[8] ABSTRACT:
A multi-zone audio distribution amplifier system includes provisions for several stereo amplifiers which may be used as master and slaveable amplifier units. The system is enclosed in a housing having a front panel with windows for displaying a set of LED display circuits on each side of the window. The housing also houses the master amplifier unit and the slave units. Each master amplifier unit includes a printed circuit board for an amplification circuit, a heat sink, and a loop-back port for connecting the amplifier units. An interface board includes a serial bus controller and a power converter circuit for receiving main ground circuit board edge and for providing power to each of the amplifier units. Each amplifier unit is operable in dependence of the others, and the slaveable amplifier may be selected by electrically connecting the amplifier units via the loop-back ports.

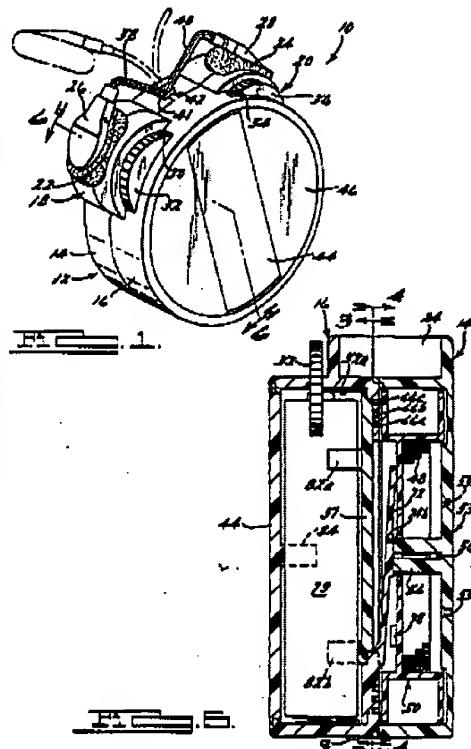
[9] 30 Claims, 6 Drawing Sheets



DOCUMENT-IDENTIFIER: US 5339461 A
TITLE: Compact radio frequency receiver having take-up
spool housed earphone
conductors

DEPR:
With still further reference to FIG. 2, the printed
circuit board 51 of the
present invention 10 can be seen to fit nestably within
the ratchet housing
section 16 against outer surface 70. The printed
circuit board 51 includes an
FM stereo receiver/amplifier circuit 51a mounted
thereon, which generally
comprises an FM stereo receiver chip 51a-1, an FM
stereo decoder chip 51a-2 and
an audio amplifier chip 51a-3. These components are
available from the Philips
Corporation under part numbers TDA7021T, TDA7041O and
TDA7051O respectively.
The printed circuit board 51 further includes a
notched portion 80 which fits
over the base portion 72a of the ratchet arm 72 when
assembled within the
ratchet housing section 16.

U.S. Patent Aug. 16, 1994 Sheet 1 of 6 5,339,461



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L15: (23) [vertical ad... | US 6081000 A | Tag: S | Doc: 7/23 | Format ...

DOCUMENT-IDENTIFIER: US 6081000 A

TITLE: AlAs oxide insulating layer between a conductive III-V substrate and an optoelectronic semiconductor device and method of manufacturing thereof

ORPL:

MacDougal et al., "Ultralow Threshold Current Vertical-Cavity Surface-Emitting Lasers with AlAs Oxide -GaAs Distributed Bragg Reflectors", IEEE Photonics Technology Letters, No. 3, Mar. 1995, pp. 229-231.

United States Patent 6,081,000
Lell

Patent Number 6,081,000
Date of Patent Jun. 27, 2000

AlAs OXIDE INSULATING LAYER BETWEEN A CONDUCTIVE III-V SUBSTRATE AND AN OPTOELECTRONIC SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF

Inventor: Alfred Lell, Münster, Germany

Assignee: Element Technologies, Inc., Münster, Germany

Appl. No.: 08/858,573
PCT Int'l. Appl. No.: PCT/DE97/03036
PCT Int'l. filing date: Sep. 11, 1997
PCT Int'l. Publ. No.: WO98/12664
PCT Int'l. Publ. date: Apr. 1, 1998

Priority Application Priority Data
Sep. 27, 1996 (DE) Germany 1996 102 40 009
Int'l. Cl.: C37B 5/30
C11G 1/10
Field of Search: 377/23, 377/47, 377/22, 377/29, 377/31, 377/45, 377/46, 377/48, 377/50, 377/52, 377/54, 377/56, 377/58, 377/60, 377/62, 377/64, 377/66, 377/68, 377/70, 377/72, 377/74, 377/76, 377/78, 377/80, 377/82, 377/84, 377/86, 377/88, 377/90, 377/92, 377/94, 377/96, 377/98, 377/100, 377/102, 377/104, 377/106, 377/108, 377/110, 377/112, 377/114, 377/116, 377/118, 377/120, 377/122, 377/124, 377/126, 377/128, 377/130, 377/132, 377/134, 377/136, 377/138, 377/140, 377/142, 377/144, 377/146, 377/148, 377/150, 377/152, 377/154, 377/156, 377/158, 377/160, 377/162, 377/164, 377/166, 377/168, 377/170, 377/172, 377/174, 377/176, 377/178, 377/180, 377/182, 377/184, 377/186, 377/188, 377/190, 377/192, 377/194, 377/196, 377/198, 377/200, 377/202, 377/204, 377/206, 377/208, 377/210, 377/212, 377/214, 377/216, 377/218, 377/220, 377/222, 377/224, 377/226, 377/228, 377/230, 377/232, 377/234, 377/236, 377/238, 377/240, 377/242, 377/244, 377/246, 377/248, 377/250, 377/252, 377/254, 377/256, 377/258, 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File Edit View Tools Window Help

DOCUMENT-IDENTIFIER: US 6075804 A
TITLE: Semiconductor device having an oxide defined aperture

BSPR:
It is another object of the invention to provide a
vertical-cavity
surface-emitting laser which utilizes the oxide -formed
aperture.

United States Patent No.
Deppe et al.

15015175944
111 Patent Number: 6,075,804
45 Date of Patent: Jun. 13, 2000

- [14] SEMICONDUCTOR DEVICE HAVING AN OXIDE DEFINED APERTURE

[15] Inventor: Daniel C. Dugay, Aspin Tech., Jack E. Zevitz, Seattle, Wash.

[16] Assignee: Philips Electronics, Eindhoven, Netherlands

[17] Appl. No.: 84/110,343

[18] Date: Feb. 21, 1979

[19] U.S. Cl.: 377/24; 377/25

[20] Int'l Cl.:

[21] U.S. Cl.: 377/24; 377/25

[22] Field of Search: 377/24, 377/25, 377/26, 377/27

[23] References Cited

Fritz, R. W., "Low-Temperature Coevaporation of Si_xN_y and Various Crystalline Layers," IEEE Transactions Electron Devices, Vol. ED-17, No. 12, pp. 1221-1227 (Dec., 1970).

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Ochiai, et al., "Kinetics of Thermal Oxidation of AlAs in Wet Oxygen," Applied Physics Letters, Vol. 44, No. 12, pp. 1050-1052, Apr. 1984.

Chang, Chih-Chang, et al., "Low Threshold Buried Heterostructure Vertical Cavity Surface-Emitting Laser," Applied Physics Letters, Vol. 45, No. 15, pp. 1267-1270 (Sept. 1984).

V.5.1.1.NET DOCUMENTATION

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Proctor Eschman—Thomas M. Altaga
Anthony Eschman—Charles P. Lewis
Attorneys at Law—Patterson & Associates

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ABSTRACT

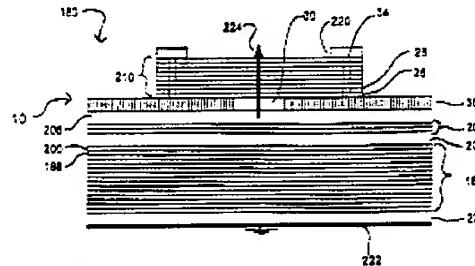
As mentioned above in section 1,

OTHER PUBLICATIONS

Chaparo, et al., "New ceramic Vitrino-Venturi-Corby Lenses Fabricated by selective Oxidation," *Electrochimica Acta*, 20, 203-204, Vol. 30, No. 14, Nov. 1985.

Chaparo, et al., "Properties and Mechanics of Selective Oxidized Vitrino-Corby Lenses," *IEEE Plasma Technology Letters*, vol. 7, No. 12, p. 1237-1239, (Nov. 1985).

Dulzono, et al., "Hydrodynamic Oxidation of Al₂O₃ An-Al₂O₃-CuOx Corby Wall Insulators and Protection," *Applied Physics Letters*, vol. 37, No. 26 pp. 2348-2354, Dec. 1980.



Details  Text  Image  KWL

 Details Text Image Full

File Edit View Tools Window Help

DOCUMENT-IDENTIFIER: US 6171982 B1
TITLE: Method and apparatus for heat-treating an SOI substrate and method of preparing an SOI substrate by using the same

ORPL:
 Y. Hayashi, et al., "Record Low-Threshold Index-Guided In GaAs/GaAlAs Vertical-Cavity Surface-Emitting Laser With A Native Oxide Confinement Structure", Electronics Letters, vol. 31, No. 7, pp. 560-562 (1995).

US 6171982 B1
 Date of Patent: Jan. 9, 2001

United States Patent

(13) United States Patent
 (14) DOCUMENT-IDENTIFIER: US 6171982 B1
 (15) Title: Method and apparatus for heat-treating an SOI substrate and method of preparing an SOI substrate by using the same

(16) Inventor: Naohiro Sato, Nagoya City, JP
 (17) Assignee: Canon Kabushiki Kaisha, Tokyu, JP
 (*) Notice: Under 35 U.S.C. 154(b), the name of this inventor shall be inserted for 3 days.

(21) Appl. No.: #09/184,418
 (22) Filed: Dec. 12, 1998
 (30) Foreign Application Priority Data
 Dec. 24, 1997, JP 11-32171
 (31) Int. Cl. H01L 21/26; H01L 2-32A;
 H01L 21/707/25
 (32) U.S. Cl. 438/790; 432/7; 432/20
 (33) Field of Search 438/795; 432/5;
 432/20
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(37) ABSTRACT

An SOI substrate having an the surface thereof a single crystal silicon film formed on an insulating substrate is heat-treated at a temperature exceeding melting temperature in order to increase the density of the single crystal silicon film and to reduce the thickness of the single crystal silicon film. The method is characterized in that the single crystal silicon film is arranged opposite to a number of annealing furnaces. This arrangement is arranged opposite to a number of annealing furnaces for heat treatment.

30 Claims, 12 Drawing Figures